A Cascaded Multilevel Inverter with Reduced Switching Devices for High Power Application

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Abstract: Multilevel inverter has become attractive in power industries and it can be applied in many applications especially on improvement of power quality. In this paper, a Cascaded H-bridge inverter (CHB) topology with reduced switch count technique is introduced. This technique reduces the number of controlled switches used in conventional multilevel inverter. To establish a single phase system, the proposed multilevel inverter requires one H-bridge and a multi conversion cell. A multi conversion cell consists of three equal voltage sources with three controlled switches and three diodes. This proposed topology also increases the level to seven with only seven controlled switches. It dramatically reduces the complexity of control circuit, cost, lower order harmonics and thus effectively reduces total harmonic distortion. Selective Harmonic Elimination (SHE) method is used to eliminate lower order harmonics. The proposed topology is suitable for any number of levels. It shows hope to reduce initial cost and complexity hence it is apt for industrial applications. Simulation work is done using the MATLAB software.

Keywords: Multilevel Inverter, Cascaded H bridge inverter, Selective Harmonic Elimination

I. INTRODUCTION

One of the most significant recent advances in power electronics is the multilevel inverter. Using this concept, the power conversion is performed with enhanced power quality. Multilevel inverter technologies have attractive features, like high voltage capability, reduced common mode voltages, near sinusoidal outputs and smaller or even no output filter, that make them suitable for use in distributed generators and high power applications [1].

Multilevel power conversion was first introduced more than two decades ago. The general concept involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. There are several advantages to this approach when compared with the conventional power conversion approach. The smaller voltage steps lead to the production of higher power quality waveforms and also reduce voltage (dv/dt) stress on the load and the electromagnetic compatibility concerns and lower total harmonic distortion, operate at high efficiencies. Another important feature of multilevel converters is that the semiconductors are wired in a series-type connection, which allows operation at higher voltages. However, the series connection is typically made with clamping diodes, which eliminates overvoltage concerns. Furthermore, since the switches are not truly series connected, their switching can be staggered, which reduces the switching frequency and thus the switching losses [2].

Multilevel inverters can be classified as shown in the fig.1. In this scenario, the diode-clamped or neutral point clamped (NPC), flying-capacitor (FC), and cascaded H-bridge (CHB) multilevel inverters were proposed to replace the traditional three-level inverters in medium- and high-voltage level applications such as motor drives and static var compensators [3]. The main drawbacks of NPC inverter topology, with a level number higher than three, is the necessity of a capacitor volt voltage across the clamped diodes. The FC multilevel inverter uses FCs as clamping devices. These topologies have several attractive properties in comparison with NPC inverters, including the advantages of the transformer less operation and redundant phase leg states that allow the switching stresses to be equally distributed between semiconductor switches. However, these inverters require excessive number of storage capacitors for high voltage steps.

Fig 1 Classification of multilevel inverter

One of the modulation strategies for these multilevel inverter topologies is the sinusoidal pulse width modulation (PWM), extended to multiple carrier arrangements of two types: level shifted (LS-PWM), also known as phase disposition, and phase shifted (PS-PWM); other established modulation methods include the multilevel space vector; and multilevel selective harmonic elimination [4].

In multiple carriers based pulse width modulation making use of several triangular carrier signals and one reference signal per phase. For an ‘m’ level inverter, m-1 carrier with the same frequency f_c and same peak-to-peak amplitude A_c are disposed such that the bands they
occupy are contiguous. The reference waveform has peak-to-peak amplitude \( A_m \) and frequency \( f_m \) and it is centered in middle of the carrier set. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is lower than a carrier signal, then the active device corresponding to that carrier is switched off. There are three types of level shifted pulse width modulation. One is alternative phase opposition disposition, where each carrier band is shifted by 180° from the adjacent bands; other is phase opposition disposition, where the carriers above the zero reference are in phase, but shifted by 180° from those carriers below the zero reference; and the third one is in-phase disposition, where all the carriers are in phase.

II. CASCaded H-BRIDGE multilevel INVERTER

Cascaded multilevel inverters synthesize a medium voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Due to these features, the cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market.

A basic structure of a cascaded multilevel inverter is shown in Fig.2. Each inverter uses a dc-link voltage to generate a modulated voltage at the output terminals. The total output voltage is obtained by the sum of each individual output voltage as shown in Fig.3. Each inverter is able to produce three output voltage levels, namely, \( +V_{dc}, -V_{dc} \) and 0 by different combinations of four switches \( S_1, S_2, S_3, S_4 \). The maximum number of voltage levels of the phase voltage \( L_{ph} \) is given by

\[
L_{ph} = 2N + 1
\]

where \( N \) is the number of inverters.

![Fig 2 Cascaded H–bridge multilevel inverter](image)

Each inverter requires an isolated dc voltage which is usually obtained by an arrangement of three-phase or single-phase rectifiers, as shown in Fig.2, and a multipulse transformer which provides the electrical isolation. In some applications, these dc voltages can be obtained directly by isolated dc sources, for example, photovoltaic panels or dc/dc isolated converters or super capacitors or fuel cells.

Cascaded H-bridge multilevel inverters typically use IGBT or MOSFET switches. These switches have low block voltage and high switching frequency. A seven level cascaded H-bridge inverter requires twelve switches and three dc sources.

![Fig 3 Seven level output voltage of cascaded H-bridge multilevel inverter](image)

The main drawback of conventional cascaded H-bridge multilevel inverter is increase in the number of main switches when the number of voltage levels increases and also needs a separate DC source for each of H-bridge. Which results more voltage stress on switches, complexity of circuit and control becomes difficult. Thus overall cost of the system increases.

III. PROPOSED TOPOLOGY

The main objective is to improve the quality of output voltage of the multilevel inverter with reduced number of switches. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the voltage with fundamental frequency.

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency waveform in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology. In this topology which separates the output voltage into two
parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency. The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. Fig. 4 shows proposed power circuit for seven level output voltage.

![Fig 4 Proposed power circuit for seven level output voltage](image)

In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities. This proposed topology also increases the level to seven with only seven controlled switches. It dramatically reduces the complexity of control circuit, cost, lower order harmonics and thus effectively reduces total harmonic distortion. It also require three dc voltage sources as in the case of conventional cascaded H-bridge multilevel inverter.

There are three modes of operation for the proposed seven-level multilevel inverter. These modes are explained as below.

**Powering Mode**: This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is $V_{dc}$, the current pass comprises; the upper supply, $Q_1$, load, $Q_2$, $D_1$, $D_2$ and $S_1$ and back to the upper supply. In the negative half cycle, $Q_1$ and $Q_2$ are replaced by $Q_3$ and $Q_4$ respectively. When the output voltage is zero, all the switches will be off and all the diodes will be on.

**Free-Wheeling Mode**: Free-wheeling modes exist when one of the main switches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; $Q_1$, load, and $D_2$, or $Q_2$, load, and $D_3$, while in the negative half cycle the current pass includes $Q_3$, load, and $D_2$ or $Q_4$, load, and $D_3$.

**Regenerating Mode**: In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice versa, where the output voltage is zero. The positive current pass comprises; load, $D_2$, $S_1$, the lower source, and $D_3$, while the negative current pass comprises; load, $D_1$, $S_1$, the lower source, and $D_4$.

The switching table for modified cascaded multilevel inverter is shown in Table I. It depicts that for each voltage level, only one of the switches is in ON condition among the paralleled switches. Multi conversion cell converts DC voltage into a stepped DC voltage, which is outputted as a stepped or approximately sinusoidal AC waveform by the H-bridge inverter. In this H-bridge, for positive half cycle, switches $Q_1$ and $Q_2$ will be turned on, similarly for negative half cycle switches $Q_3$ and $Q_4$ must be in ON condition.

![Table I. Basic Operation of Proposed Topology](table)

<table>
<thead>
<tr>
<th>S. N.</th>
<th>Multi-Conversion Cell</th>
<th>H-Bridge</th>
<th>Volt Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ON Switches</td>
<td>OFF Switches</td>
<td>ON Switches</td>
</tr>
<tr>
<td>1</td>
<td>$S_1,S_2,S_3$</td>
<td>$D_1,D_2,D_3$</td>
<td>$Q_1,Q_2$</td>
</tr>
<tr>
<td>2</td>
<td>$S_1,S_2,D_3$</td>
<td>$S_3,D_1,D_2$</td>
<td>$Q_1,Q_2$</td>
</tr>
<tr>
<td>3</td>
<td>$S_1,D_2,D_3$</td>
<td>$S_2,S_3,D_1$</td>
<td>$Q_1,Q_2$</td>
</tr>
<tr>
<td>4</td>
<td>$D_1,D_2,D_3$</td>
<td>$S_1,S_2,S_3$</td>
<td>$Q_1,Q_2$</td>
</tr>
<tr>
<td>5</td>
<td>$S_1,S_2,S_3$</td>
<td>$D_1,D_2,D_3$</td>
<td>$Q_3,Q_4$</td>
</tr>
<tr>
<td>6</td>
<td>$S_1,S_2,D_3$</td>
<td>$S_3,D_1,D_2$</td>
<td>$Q_3,Q_4$</td>
</tr>
<tr>
<td>7</td>
<td>$S_1,D_2,D_3$</td>
<td>$S_2,S_3,D_1$</td>
<td>$Q_3,Q_4$</td>
</tr>
</tbody>
</table>

The $S$ number of DC sources or stages and the associated number output level can be calculated by using the equation as follow

$$m = 2S + 1$$
The number of main switch required can be calculated as

\[ N_s = \frac{m-1}{2} + 4 \]

Therefore, in order to produce a seven level output voltage the proposed cascaded H-bridge multilevel inverter uses three dc voltage sources and seven main switches.

IV. MODULATION TECHNIQUE

There are number of modulation control techniques such as sinusoidal PWM method (SPWM), space vector PWM method (SVPWM), selective harmonic elimination method (SHE), and active harmonic elimination method, and they all can be used for inverter modulation control. For the proposed inverter control, a sensible modulation control method is the fundamental frequency switching control for high output voltage and Sinusoidal PWM control for low output voltage. In this paper, fundamental frequency switching control is used in H-bridge MLI. The multilevel PWM inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages in stepped waveform. The commutation of the switches allows the addition of the capacitor voltages which reaches the high voltage level at the output, while the power semiconductors withstand only with reduced voltage. A single phase leg of inverter with different numbers of levels by which the action of the power semiconductors is represented by an ideal switch with several positions. A seven-level PWM inverter generates an output voltage with seven values (levels) with respect to the negative terminal of the capacitor.

Alternate Phase Opposition Disposition (APOD)

Alternative Phase Opposition Disposition modulation technique is used in the proposed topology. In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbour carrier by 180 degree. For m level, (m-1) carrier waves are used. Each carrier wave has equal magnitude and frequency. These waves are compared with a reference wave. If reference is greater than a carrier set, then the active switch corresponding to that carrier set is turned on. Otherwise the corresponding switch is turned off.

For ‘m’ level inverter, modulation index

\[ m_a = \frac{A_m}{(m-1) \times A_c} \]

Frequency modulation \[ m_f = \frac{f_c}{f_m} \]

The rules for APOD method, when the number of level \( m = 7 \), are

1. The \( m - 1 = 6 \) carrier waveforms are arranged so that every carrier waveform is in out of phase with its carrier by 180°. The converter switches to \( +1 \ V_{dc} \) when the reference is less than two uppermost carrier waveform and greater than all the other carrier waveforms.
2. The converter switches to \( 2 \ V_{dc} \) when the reference is less than the uppermost carrier waveform and greater than all other carriers.
3. The converter switches to \( 3 \ V_{dc} \) when the reference is greater than all the carrier waveforms.
4. The converter switches to 0 when the reference is less than the three uppermost carrier waveform and greatest than lowermost carrier.
5. The converter switches to \( -1 \ V_{dc} \) when the reference is greater than the two lowermost carrier waveform and lesser than all other carriers.
6. The converter switches to \( -2 \ V_{dc} \) when the reference is lesser than all the carrier waveforms and greater than the lowermost waveform.
7. The converter switches to \( -3 \ V_{dc} \) when the reference is less than all the carrier waveforms.

V. SIMULATION RESULTS

The performance of the proposed converter and the control strategy are evaluated by conducting the Simulation analysis of the system using MATLAB/Simulink version R2011a. MATLAB is a high-level language and interactive environment that facilitates to perform computationally intensive tasks faster than with traditional programming languages such as C, C++, and Fortran. Simulink® is an environment for multi-domain simulation and model-based design for dynamic and embedded systems. It provides an interactive graphical environment and a customizable set of block libraries that enables to design, simulate, implement, and test a variety of time-varying systems, including communications, controls, signal processing etc.

The performance of the proposed cascaded multilevel inverter is verified through the simulation results. Fig.5 shows the simulation diagram of proposed configuration using MATLAB. Simulation parameters are given in the table II.
Each input dc voltage source is 85V in order to produce an output voltage of 230V. Each input dc voltage of proposed multilevel inverter is obtained by a boost converter with input dc voltage of 24 V. Simulation diagram of a boost converter is shown in Fig.6.

Fig 6 Simulation diagram of boost converter

The 230V DC is converted into 230V AC at fundamental frequency by the seven level inverter. Simulation diagram of the control circuit is given in the fig.7. Since it is a 7-level inverter, the number of carriers required is six. Each carrier are arranged in a level shifted manner where the positive side carrier and reference is compared to get the gating pulse for the period of 0 to π whereas negative side carrier and reference are compared to get the gating pulse for a period of π to 2π. This is then applied to the corresponding switches.

Fig 7 Simulation Diagram For Control Circuit

Simulation results are shown in the following figures. The gating signals for each switches is given in the fig.8, fig. 9 and fig.10.

DC voltage of 24 V is given to the input of boost converter. Which boost this input voltage to 85 V. The input and output voltage waveforms of the boost converter is shown in fig.11 and fig.12.

Fig 8 Gate Signals For The Switches Q1 And Q2

Fig 9 gate signals for the switches Q3 and Q4

Fig 10 Gate Signals For The Switches S1, S2 And S3

Fig 11 Input Voltage Waveform of Boost Converter

Fig 12 Output Voltages Waveform of Boost Converter
The voltage and current waveforms of proposed multilevel inverter with a resistive load of 100Ω are shown in fig.13 and fig.14. The resulting THD for current is 18.32% which is shown in the fig.15.

Fig 13 Seven Level Output Voltage Waveform of Proposed Topology

Fig 14 Seven Level Output Current Waveform of Proposed Topology

Fig 15 Waveform of THD Analysis of Output Voltage

<table>
<thead>
<tr>
<th>Simulation Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Voltage</td>
<td>85 V</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>5KHz</td>
</tr>
<tr>
<td>Modulation Index</td>
<td>0.6</td>
</tr>
<tr>
<td>Frequency Modulation</td>
<td>40</td>
</tr>
<tr>
<td>Load Resistance</td>
<td>100Ω</td>
</tr>
<tr>
<td>Boost Converter</td>
<td></td>
</tr>
<tr>
<td>Switching frequency</td>
<td>50KHz</td>
</tr>
<tr>
<td>Capacitor</td>
<td>5000μF</td>
</tr>
<tr>
<td>Inductor</td>
<td>200mH</td>
</tr>
</tbody>
</table>

VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper revealed that proposed modified multilevel inverter topology with reduced number of switches can be implemented for industrial drive applications. This multilevel inverter structure and its basic operations and control scheme have been discussed elaborately. By controlling the modulation index, the desired number of levels of the inverter’s output voltage can be achieved. As conventional seven level inverter involves twelve switches, it increases switching losses, cost and circuit complexity. The proposed inverter engages only seven switches with three diodes, which reduces switching losses, cost and circuit complexity. A comparison of conventional seven level inverters with the proposed seven-level inverter is shown in the table III.

Table III. Comparison of Seven-Level Inverter

<table>
<thead>
<tr>
<th>Multilevel Inverter Type</th>
<th>Diode Clamped</th>
<th>Flying Capacitor</th>
<th>Cascaded H-Bridge</th>
<th>Proposed Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of main switches</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>7</td>
</tr>
<tr>
<td>Number of clamped diodes</td>
<td>30</td>
<td>Nil</td>
<td>Nil</td>
<td>Nil</td>
</tr>
<tr>
<td>Number of clamped capacitors</td>
<td>Nil</td>
<td>2</td>
<td>Nil</td>
<td>Nil</td>
</tr>
<tr>
<td>Number of voltage split capacitors</td>
<td>6</td>
<td>Nil</td>
<td>Nil</td>
<td>Nil</td>
</tr>
<tr>
<td>High frequency switching device</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>3</td>
</tr>
</tbody>
</table>

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VII. REFERENCES


