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# Comparative Analysis of Various PWM Strategies for Single Phase Seven Level Asymmetrical Modified Quasi Z Source Multilevel Inverter with Voltage Lift Cell

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***Abstract:*** ***This paper presents performance analysis of various PWM strategies for the chosen single phase seven level bipolar asymmetrical Modified Quasi z source cascade H bridge inverters with voltage enhancement technique. Simulation using MATLAB-SIMULINK is performed with bipolar triangular fixed amplitude multi-carrier PD, APOD, POD PWM strategies with rectified sine wave reference and trapezoidal reference for the chosen Z-Source MLI with modified CHB. For a wide range of shoot through duty ratios, the peak value and root mean square value of the fundamental component and THD of the output voltage are evaluated with different modulation indices. This paper presents significantly improved results to produce great boosting in the root mean square value of the fundamental component with enriched voltage enhancement techniques along with suitable PWM strategy.***

***Keywords: Multi-Level Inverter, H-Bridge, Quasi Z Source, Shoot Through Duty Cycle, , Voltage Lift (VL), Pulse Width Modulation.***

## I. INTRODUCTION

In recent years, various industrial applications require high power apparatus. Some utility applications and motor drives need medium voltage and megawatt power. It is problematic to connect only one power semiconductor switch directly for a medium voltage grid. Hence, a multilevel power inverter configuration has been introduced [1]-[3]. Apart from achieving high power ratings, multilevel inverter also permit us the use of renewable energy resources like wind, photovoltaic, fuel cells etc[4].

Among different multilevel converters topologies, the cascaded multilevel H bridge converter plays an exceptional priority due to its simple and modesty control. From separate DC sources, it utilizes full H-Bridges connected is series to produce inverted AC. when compared to other conventional inverters, diminution in this topology is a greatest advantage due to reduction in number of devices used. The output is fairly sinusoidal in nature without filter. In this structure Soft-switching can be used to avoid lossy and bulky resistor capacitor-diode snubbers. For high power applications, it is a favorable structure as it provides higher voltage at higher modulation frequencies with a low switching (carrier) frequency. It means for the same THD, low switching loss [5],[8].

When two switches of the same-phase leg is switched ON at the same time in a traditional voltage source inverter (VSI) due to short circuit (shoot through of current), switches might get destroyed. The maximum inverter output voltage (Vpeak) can never exceed the dc bus voltage. A train of square wave voltage waveforms with different duty ratio is generated by Inverter. Z-source inverter (ZSI) helps to overcome all these limitations [9]. The reliability of inverter is significantly improved because the shoot through due to Electro Magnetic Interference (EMI) noise can no longer destroy the circuit. ZSI is cheaper and consists of active state and shoot through state [7]. In ZSMLI, the input DC voltage can be bucked or boosted by properly adjusting the shoot through time period of pulses. The THD in the output voltage is limited by appropriate selection of firing pulses in ZSMLI.

The passive components of Quasi Z source are sketched in a way to yield a maximum boost capability with less number of switches, in turn leads to an efficient system. Its unique features are boost capability and single stage voltage inversion [6]. For the generation of shoot through states many modulation strategies are available. For the proposed Quasi Z-source multilevel inverter (QZMLI), simple boost control technique is used [11], [13]. The shoot through is added to the pulse width modulation so as to achieve voltage boost [10].

## II. PROPOSED TOPOLOGIES

For the proposed modified asymmetrical QZ source CHB MLIs having voltage lift cells, simulation using MATLAB-SIMULINK is performed with bipolar triangular fixed amplitude multi-carrier alternate Phase opposition disposition(APOD), Phase opposition disposition (POD) ,Phase Disposition (PD) PWM strategies with rectified sine wave reference and trapezoidal reference. The performance indices, peak value and root mean square value of the fundamental component and THD of the output voltage are evaluated and compared for various modulation indices for the chosen inverter topologies. This paper provides the results of simulation using MATLAB-SIMULINK for multi-carrier PWM strategies [15]-[18] the following chosen topologies of cascaded H Bridge MLI namely Bipolar Asymmetrical Modified quasi Z source MLI having Voltage Lift (VL) cells.

To identify PWM technique with best performance for the proposed topologies, the following PWM strategies for the proposed MLI is carried out.

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1. Bipolar triangular fixed amplitude multi-carrier Phase Disposition (PD) PWM with rectified sine reference.
2. Bipolar triangular fixed amplitude multi-carrier Phase Opposition Disposition (POD) PWM with rectified sine reference.
3. Bipolar triangular fixed amplitude multi-carrier Alternative Opposition Disposition (APOD) PWM with rectified sine reference.
4. Bipolar triangular fixed amplitude multi-carrier Phase Disposition (PD) PWM with trapezoidal reference.
5. Bipolar triangular fixed amplitude multi-carrier Phase Opposition Disposition (POD) PWM with trapezoidal reference.
6. Bipolar triangular fixed amplitude multi-carrier Alternative Opposition Disposition (APOD) PWM with trapezoidal reference.

## III. ASYMMETRIC MODIFIED QUASI Z SOURCE MLI HAVING VOLTAGE LIFT CELLS

The proposed asymmetric voltage-lift qZ-Source fed MCHB seven level inverter topology consists of three voltage sources, nine diodes, nine equal valued inductors, nine equal valued capacitors and three half H-bridge cells cascaded with a full H-bridge cell . Replacement of inductor L2 in qZS-network by VL cell results in asymmetric VL-qZS-MCHB seven level inverter .One port of the asymmetric VL-qZ-Source network-1 is connected to the voltage source Vin1 and the other port of the qZ network-1 is connected to the half H-bridge cell-1. This half H-bridge cell-1 consists of two switches Sa1 and Sa2 connected in series in the same leg. The midpoint of the half H-bridge cell-1 is connected to the top common point of full H-bridge circuit. The bottom point of the half H-bridge cell-1 is connected to the mid-point of the half H-bridge cell-2. Similarly the other asymmetric VL-qZ-Source network fed half H-bridge cell-2 and half H-bridge cell-3 are cascaded with full H-bridge cell to provide seven level output voltage. The common full H-bridge cell consists of two legs namely first leg and second leg. Two switches S1 and S4 connected in series in the first leg. Similarly the switches S3 and S2 are connected in series in the second leg. The midpoints of both legs of the common full H-bridge are connected to the load. The operating principles of the proposed topology is explained by shoot-through state and non-shoot-through state. The equivalent circuits of the shoot-through state and non-shoot-through state of are as shown in Fig 3.2 and Fig 3.3. The below equation provides formula for boost factor $B = \frac{2}{1-3D_{sh}}$

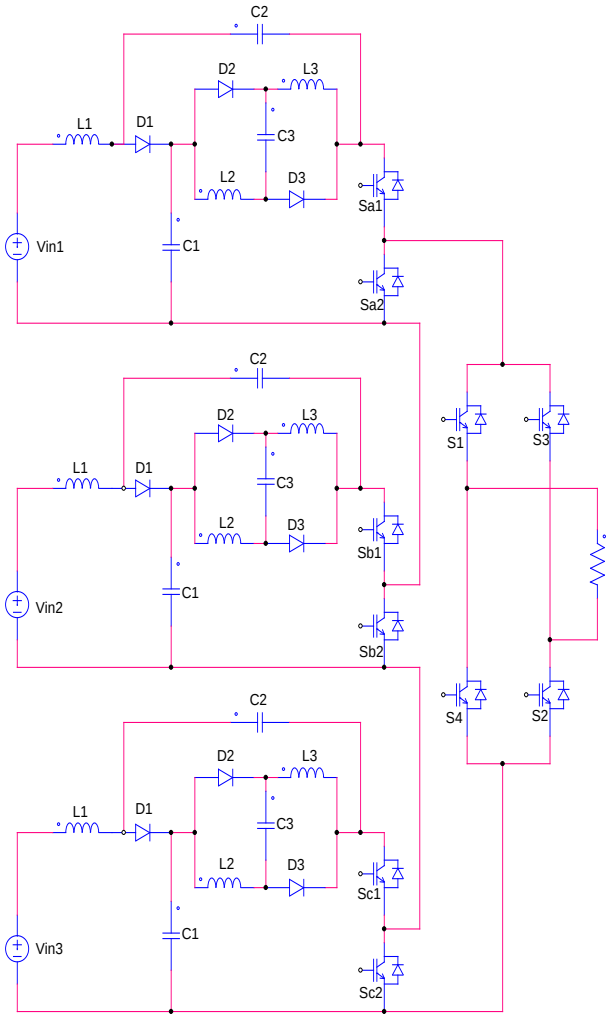


Fig 3.1. Configuration of Single Phase Seven Level Asymmetric VL QZ Source Fed Modified CHB Inverter

The operating principles of the proposed topology seven level asymmetrical modified cascaded quasi Z-Source H-bridge inverter with voltage lift cells can be easily understood by the shoot-through state and non- shoot-through states. The equivalent circuit of the shoot-through state and non-shoot-through state are shown in Fig.3.2 and Fig.3.3.

*Shoot-Through State:*

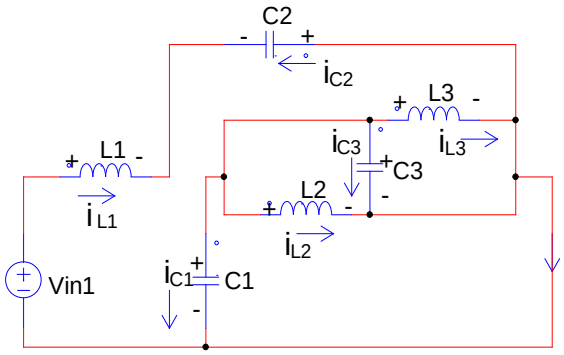


Fig. 3.2. Shoot-Through State of Proposed Asymmetrical VL QZ Network Fed CHB MLI Topology

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The equivalent circuit of the shoot-through mode of proposed circuit in Fig.3.2. With reference to the Fig 3.2 . L2, L3 and C3 are connected in parallel where the diodes D2 and D3 are on and D1 is off. The capacitor C3 is charged while C1 and C2 are discharged. All the inductors L1, L2 and L3 store energy during this state.

*Non Shoot-Through State:*

The equivalent circuit of the non-shoot through mode of proposed circuit in Fig.3.3 .In this mode,, L2, L3 and C3 are connected in series where the diodes D2 and D3 are off and D1 is on. The capacitor C3 is discharged, while C1 and C2 are charged. All the inductors L1, L2 and L3 transfer energy from the dc voltage source to the load during this state.

Shoot-through Duty Ratio, $D_{Sh} = \frac{T_O}{T}$

Where To is the duration of shoot-through zero state, T is the switching cycle

Modulation index , $M = 1 - D_{Sh}$

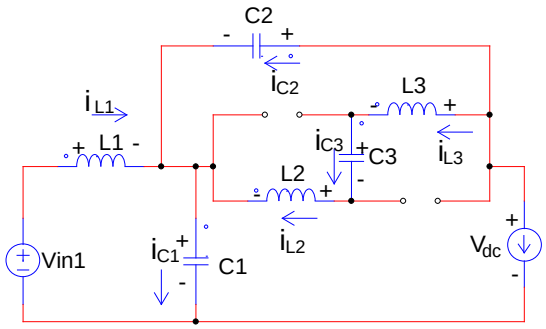


Fig. 3.3. Non Shoot-Through State of Proposed Asymmetrical VL QZ Network Fed CHB MLI Topology

The simulation using MATLAB-SIMULINK is performed for various shoot-through duty ratios with bipolar triangular fixed amplitude multi-carrier alternate Phase opposition disposition(APOD), Phase opposition disposition (POD) ,Phase Disposition (PD) PWM strategies with rectified sine wave reference for the newly developed asymmetrical configuration of modified Z source CHB MLIs having voltage lift cell only in the top arm of the Z-Source network.

To identify PWM technique with best performance for the proposed topology, the following PWM strategies is carried out.

1. Bipolar triangular fixed amplitude multi-carrier Phase Disposition (PD) PWM with rectified sine reference.
2. Bipolar triangular fixed amplitude multi-carrier Phase Opposition Disposition (POD) PWM with rectified sine reference.
3. Bipolar triangular fixed amplitude multi-carrier Alternative Opposition Disposition (APOD) PWM with rectified sine reference.
4. Bipolar triangular fixed amplitude multi-carrier Phase Disposition (PD) PWM with trapezoidal reference.
5. Bipolar triangular fixed amplitude multi-carrier Phase Opposition Disposition(POD)PWM with trapezoidal reference.
6. Bipolar triangular fixed amplitude multi-carrier Alternative Opposition Disposition (APOD) PWM with trapezoidal reference.

## IV. Simulation Results And Analysis

The Simulation study using MATLAB software is carried for both the proposed topologies. The circuit parameters for simulation are as follows: $L_1$=$L_2$=$L_3$= 40 m H and $C_1$=$C_2$=6000 µF. Switching frequency $f_s$ = 5kHz.The input voltage $V_{in1}$=$V_{in2}$=$V_{in3}$ = 100V and R load = 50 Ω. The important performance indices namely $V_{rms}$(fundamental),Vpeak (fundamental ) and %THD of simulated output voltage for $D_{sh}$ = 5%,10% and 15% are noted down .

With bipolar triangular fixed amplitude multi-carrier alternate Phase opposition disposition(APOD), Phase opposition disposition (POD) ,Phase Disposition (PD) PWM strategies with rectified sine wave reference and trapezoidal reference for the newly developed asymmetrical configuration of modified Z source CHB MLIs having voltage lift cell is carried out.

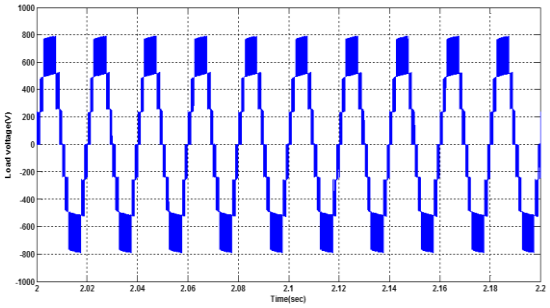


Fig. 4.1. Simulated Output Voltage Waveform of Asymmetric VL QZ Source fed MCHB Seven Level Inverter POD (Dsh = 10%)

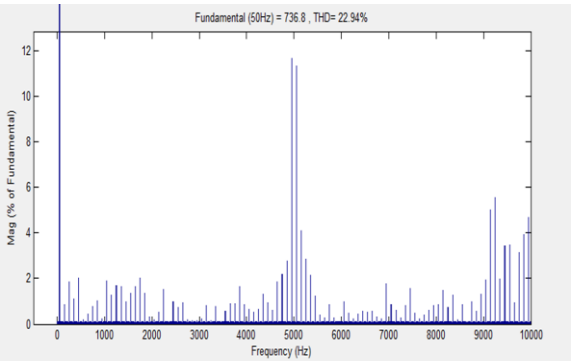


Fig. 4.2. FFT plot of Simulated Output Voltage of Asymmetric VL QZ Source fed MCHB Seven Level Inverter POD (Dsh = 10%)

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The sample output voltage waveforms and the corresponding FFT plot for asymmetric VL-QZ-Source fed MCHB with Phase opposition disposition (POD) PWM strategies with rectified sine wave reference and shoot through duty ratio $D_{sh}$ = 10% is showed in the figure 4.1and 4.2

The sample output voltage waveforms and the corresponding FFT plot for asymmetric VL-QZ-Source fed MCHB with alternate Phase opposition disposition (APOD) strategies with trapezoidal reference and shoot through duty ratio $D_{sh}$ = 5% is showed in the figure 4.3 and 4.4.

The important performance indices namely $V_{rms}$(fundamental) and %THD of simulated output voltage for $D_{sh}$ = 5%,10% and 15% is as tabulated below in Table 4.1 and 4.2.

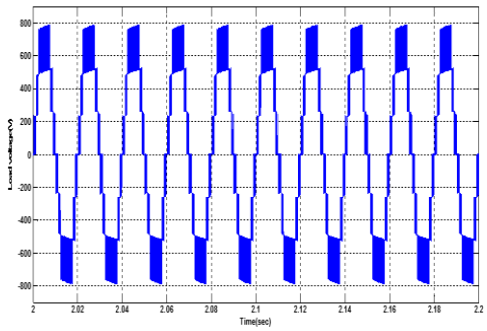

Fig. 4.3. Simulated Output Voltage Waveform of Trapezoidal Reference Asymmetric VL QZ Source Fed MCHB Seven Level Inverter APOD (Dsh = 5%)

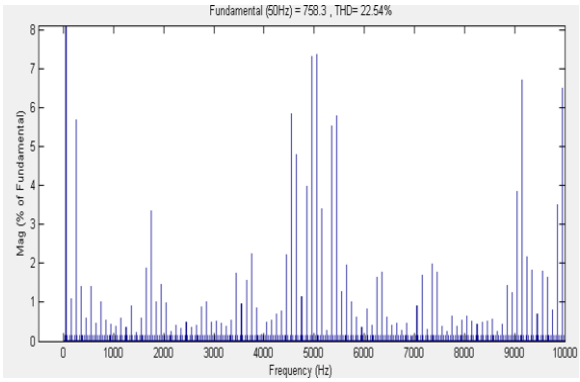


Fig. 4.4. FFT Plot of Simulated Output Voltage of Trapezoidal Reference Asymmetric VL QZ Source Fed MCHB Seven Level Inverter APOD (Dsh = 5%)

Table 4.1. Performance Indices of Asymmetric VL QZ Source Fed MCHB Seven Level Inverter with Sine Reference and Triangular Carrier

| | MCHB( SINE –TRI) | | | | | |
|---|---|---|---|---|---|---|
| | $D_{SH}$ =5% | | $D_{SH}$ =10% | | $D_{SH}$ =15% | |
| | $V_{rms}$(V) | THD(%) | $V_{rms}$(V) | THD(%) | $V_{rms}$(V) | THD(%) |
| APOD | 509.7 | 22.69 | 519.7 | 23.05 | 515.6 | 23.28 |
| PD | 507.9 | 22.93 | 519.8 | 22.20 | 515.8 | 23.43 |
| POD | 509.1 | 23.19 | 521 | 22.94 | 517 | 23.18 |

Table 4.2. Performance Indices of Asymmetric VL QZ Source Fed MCHB Seven Level Inverter with Trapezoidal Reference and Triangular Carrier

| | MCHB (TRAPEZ-TRI) | | | | | |
|---|---|---|---|---|---|---|
| | $D_{SH}$ =5% | | $D_{SH}$ =10% | | $D_{SH}$ =15% | |
| | $V_{rms}$(V) | THD(%) | $V_{rms}$(V) | THD(%) | $V_{rms}$(V) | THD(%) |
| APOD | 536.9 | 22.54 | 535.6 | 22.6 | 533.3 | 22.56 |
| PD | 533.8 | 22.96 | 533.1 | 23.04 | 529.9 | 23.03 |
| POD | 536.6 | 22.74 | 535.9 | 22.80 | 532.7 | 23.06 |

The simulation results affirm the development of the various PWM strategies for the chosen single phase seven level bipolar asymmetrical Modified Quasi z source cascade H bridge inverter with voltage enhancement technique. The above simulation results also indicate that asymmetric QZ-Source fed MCHB seven level inverter along with s voltage enhancement technique performs better with bipolar triangular fixed amplitude multi-carrier APOD PWM strategies with trapezoidal reference along with Dsh = 5% itself than any other proposed PWM combination strategies.

## V. CONCLUSION

The simulation results affirm the development of the various PWM strategies for the chosen single phase seven level bipolar asymmetrical Modified Quasi z source cascade H bridge inverter with voltage enhancement technique. The above simulation results also indicate that asymmetric QZ-Source fed MCHB seven level inverter along with voltage enhancement technique performs better with bipolar triangular fixed amplitude multi-carrier APOD PWM strategies with trapezoidal reference along with Dsh = 5% itself than any other proposed PWM combination strategies.

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