International Journal of Electrical Electronics & Computer Science Engineering
Volume 5, Issue 1 (February, 2018) | E-ISSN : 2348-2273 | P-ISSN : 2454-1222
Available Online at www.ijeecse.com

A Review on Instrumentation Amplifier and Methods to Improve CMRR

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Abstract: ***Many bio signals are encountered in day to day lifewhich can be measured by using an electrode. Therefore, to measure these signals electrodes are placed in contact with human body so that these signals can be converted into electrical signals. But these signals are of less amplitude i.e. few milivolts and they acquire unwanted noise signals from the surroundings. It is required to suppress these unwanted noise signals as well as to amplify these low magnitude signals and therefore a very large CMRR is required for that. CMRR is an important parameter in deciding the efficiency of INA, as large CMRR implies that noise factor would be very less. So this paper reviews some basic principles of the classic three op-amp instrumentation amplifier and some methods to increase CMRR so as to reduce common mode signals in low amplitude and low frequency signal.***

Keywords: CMRR (Common Mode Rejection Ratio), INA (Instrumentation Amplifier), OA (Operational Amplifier), DC Offset, Current Mirrors (CM).

I. INTRODUCTION

Instrumentation amplifiers (INAs) are used in many industries and medical field also to amplify small signals and to remove noise factor from them. The bio signals to be recorded or measured by using electrode are amplified using instrumentation amplifier. As it is the first block of any analog system therefore plays a vital role to improve various parameters like noise level and CMRR (Common mode rejection ratio) of overall system. High impedance and the high CMRR are two important factors which play a major role in many sensors and biometric applications for example temperature sensors, pressure sensors, different weigh scales, ECG, EEG as noise and unwanted signals can cause undesirable output. Therefore it is highly required that the INA should have large CMRR. Instrumentation amplifier will consume high power therefore the design should be made in such a way to balance noise and power both.

A. Basics of Instrumentation Amplifier:

Basic nature of having high impedance and the high common mode rejection makes instrumentation amplifier an obvious choice to be used in almost every field. The basic three op-amp instrumentation amplifier is there to minimise the common-mode voltage and then amplifies the signal. Also non –inverting inputs at the input stage are applied to increase the input impedence [3]. Saturation of the amplifier's input stage is dependent on common mode voltage (V_{CM}) and the differential voltages (V_D) and therefore can be avoided by taking care of both (V_{CM}) and (V_D) .

A saturated input stage have very bad consequences to the overall circuitry but it can be avoided by attaining maximum design margin. By using amplifiers with rail to rail input and output configurations, the saturation of input stage can be avoided. The following discussion shows the basic operation of classic three op-amp based instrumentation amplifier .Basic block diagram of instrumentation amplifier is shown in Fig 1. There are two main inputs V_{CM} and V_D where the former one is the voltage common to both inputs V_+ and V_- and is the average sum of V_+ and V_- also known as common mode voltage, latter one is the net difference of V_+ and V_- known as differential voltage.

$$V_{CM}= (V_+ + V_-)/2 \text{ and } V_D= V_+ - V_- \quad (1)$$

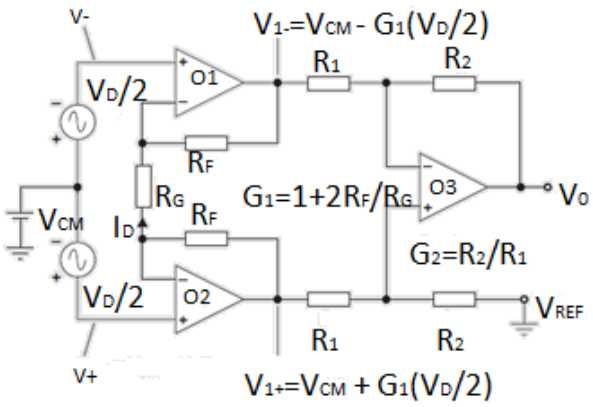

Fig. 1. Basic Instrumentation Amplifier

The node voltages on the input pins of the amplifier (V+ and V-), in terms of common mode voltage and differential voltage, are given in (2).

$$V+ = V_{CM} + V_D /2 \text{ and } V- = V_{CM} – V_D /2 \quad (2)$$

In the non-saturated mode, V_D is applied across the gain setting resistor R_G because of the resulting action of two initial op-amps and hence I_D is generated.

$$I_D = (V_+ + V_-) /R_G = V_D/R_G \quad (3)$$

The output voltages of O1 and O2 are therefore:

$$V_{1+} =V_{CM} + V_D /2 + I_D R_F \text{ and}$$

$$V_{1-}=V_{CM}-V_D/2-I_D R_F \quad (4)$$

(3) and (4) yields :

$$V_{1+} = V_{CM} + V_D G_1/2 \text{ and } V_{1-} = V_{CM} – V_D G_1/2$$

$$\text{Where } G_1 = 1+ 2R_F/R_G \quad (5)$$

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(5) shows G_1 amplifies the differential component $V_D/2$, and the common mode passes the input stage with the unity gain and is subsequently cancelled out by the common mode rejection of O3. This enables the INA to remove common mode signals from the desired signal. Hence, the signal gets amplified from 100 to 1000 times to get required sensitivity.

Now it is already discussed that the clipping of common mode signals is of much concern to get the desired output. Therefore to reduce the common mode signals, instrumentation amplifier must have high CMRR. CMRR (Common mode rejection ratio) tells how nicely the input or output can reject the unwanted signals and is given by

CMRR = A_{DM}/A_{CM} where A_{DM} is the differential gain and A_{CM} is the common-mode gain. Now here are some methods which are discussed in some research papers to improve CMRR. Basically, different approaches are adopted to make variations in the circuit diagram of INA to increase CMRR. Overall working of the INA will be same as explained earlier.

II. METHODS TO IMPROVE CMRR

1. As already mentioned that high CMRR is one of the major requirement of INA and this can be achieved using many variations in circuit diagram, one of such method to change the circuit diagram is AC coupling [9]. AC signals can be extracted by suppressing noise and dc offset which can be done using blocking capacitors as shown in Fig. 2. It is shown in the figure that AC coupled INA can be implemented using resistors and capacitors . Here R_1 and C_1 will set high cutoff frequency given by $1/(2(R1)(C1)\pi)$. All resistors are implemented with diode connected PMOS devices. To keep silicon area small, predefined pseudo resistors are used and they are biased in sub threshold region to attain high resistance. DC offset is eliminated to a large extent by this .Input stage amplifiers O1 and O2 are designed by operational amplifier and the second stage amplifier O3 is designed by miller based amplifier as shown in Figure 3.

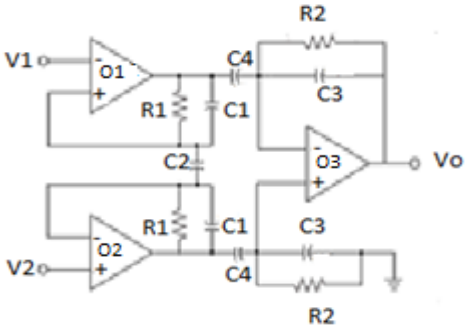

Fig. 2. AC Coupled Instrumentation Amplifier

Input voltage is converted to an output current by using balanced O1 and O2. The obtained current is proportional to the input voltages. OA has high input and output impedance which is quite useful. Maximum transfer of the source voltage to the input of OA is possible only if the OA has high input impedance. Also, high output impedance allows maximum transfer of output current to load.

The second stage amplifier is the differential amplifier as shown in Fig. 3. which is to reject the output voltages of input amplifiers, W/L ratio and other required specifications are also shown in the figure. Miller compensated op-amp have high open loop DC gain which is helpful in increasing the CMRR. CMRR obtained using this configuration increases upto 142dB.

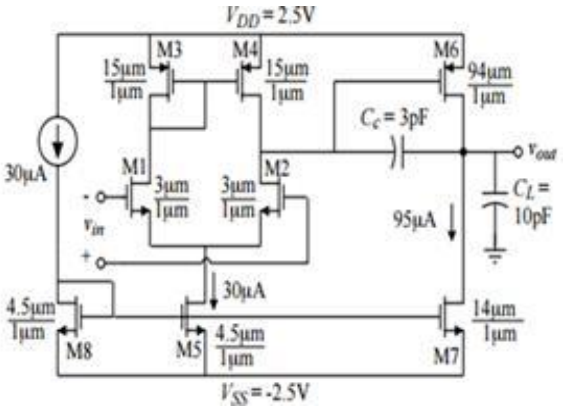

Fig. 3. Miller Compensated Amplifier

2. Here is the second method discussed to achieve low offset and high CMRR. In this NMOS transistors are used along with two phase clock system with a frequency of 20KHz.The circuit of the overall INA is shown in Fig. 4 which includes the noise suppression circuitry [3].The input voltages of the INA at positive and negative terminals are V+ and V- and Vo is provided at the output terminal. The non overlapping clock ph1 and ph2 are used which starts the NMOS transistors. Here non overlapping signifies that the product of two signals will always be zero. Capacitors are being provided between the input terminals to store the offset voltage and thereafter can be used to suppress these offset. The gain of INA without offset cancellation is given by the ratio which is expressed as

$$V_O = R_4/R_3(1+ 2R_2/R_1)(V_+ - V_-) \quad (6)$$

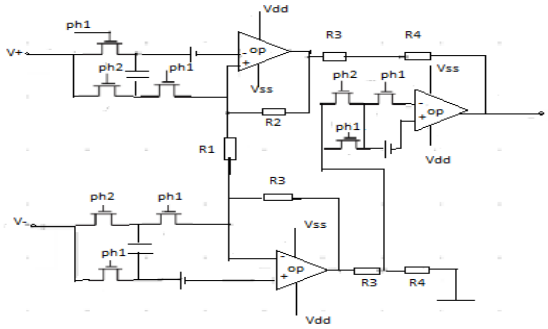

Fig. 4. Circuit Diagram of INA

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The gain of each op amp is given by the ratio of resistors across the op amp. The gain across each op amp is given by-

$$A_1 = A_2 = R_4/R_2(1+ 2R_2/R_1) \quad (7)$$

$$A_3 = -2(1+ R_4/R_3) \quad (8)$$

NMOS transistor acts like a switch and when it is closed then the switch will be in the offset storage mode and each op-amp's offset are stored across the resistor. The output stage will provide the signal which do not contain any common-mode signal resulting in high CMRR. The overall common−mode rejection ratio (CMRR) is given by:

$$CMRR = (A_{d1}A_{d2})/(A_{cm1}A_{cm2}) \quad (9)$$

Where A_{d1} and A_{d2} are the differential mode gain of first and second stage respectively and A_{cm1} and A_{cm2} are the common mode gain of first and second stage respectively.

The charges are released in the conducting channel whenever the NMOS switch is off and these charges are removed through drain and source terminals of MOS. Also, the charges which flows through substrate are generally neglected. The rest division of charges between drain and source is dependent on the ratio R. Ratio R is the total capacitance at the switch drain and at the source and on switching parameter which is calculated by transistor's "ON" Resistance, divided by the the slope of clock signal that is applied to the gate. Non overlapping clock is the main requirement in this circuit to increase CMRR. Therefore, to generate the required clock signal, the circuit is used which is shown in Fig. 5. Clock used here has frequency of 20KHz. For this, an inverter and two NOR gates are required. These clock helps in switching ON and OFF of the NMOS for storage and cancellation mode respectively.

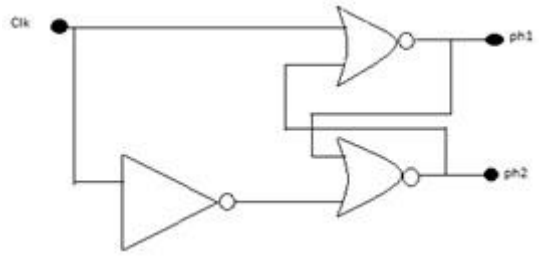

Fig. 5 Non Overlapping Clock Generation Circuit Diagram

3. As the conventional INA consists of three op-amps and many resistors. So, a good performance of INA is dependent on the resistors and a very good matching, which is difficult to achieve as resistors must be quite accurate. Eventually it leads to the increased cost of INA and therefore, to have good matching becomes difficult which lessen the CMRR. To solve this issue, the classic three op-amp based amplifier which is composed of so many resistors is replaced by a circuit which is shown in Fig. 6. The main difference in this proposed circuit is that it contains current mirrors and very few resistors along with op-amps [5].

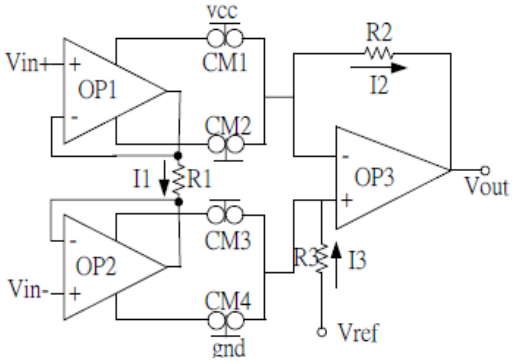

Fig. 6. Circuit Diagram of INA

The input voltage are applied at the terminals V_{in+} and V_{in-}, current (I1) will flow through R1, so

$$I_1 = (V_{in+} - V_{in-}) /R_1 \quad (10)$$

Current mirrors CM1 and CM2 are provide so that they will make sure that exact same amount of current I_1 will flow through R_2 which is named as I_2. Now, it is found that $I_1 = I_2 = -I_3$. The output voltage is specified in (XI), with the circuit of the proposed INA as shown in Figure 6.

$$V_{out} = -2 [(V_{in+}) – (V_{in-})] * R_2/R_1 \quad (11)$$

Because the signal which is sensed by the INA are weak, hence it gets affected with the noise present. Flicker noise is low frequency characteristic and therefore it is dependent on the width and length of CMOS transistors, as described in (XII). Area has to be maximised to reduce the flicker noise as it is inversely proportional to the area.

$$V_n^2 = (K/COXWL) * (1/f) \quad (12)$$

The voltage-in and current-out of the op-amp which is used in constructing INA as shown in Fig. 7.

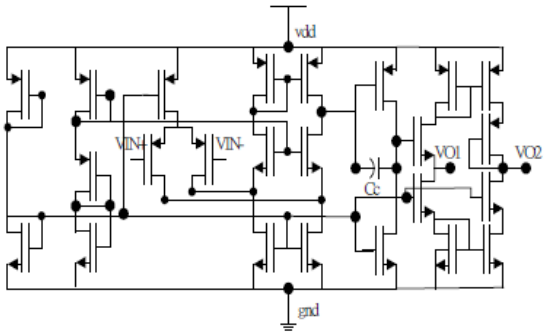

Fig. 7. Schematic Diagram of Op-Amp

Op-amp shown is consisted of four stages, the first stage is a bias circuit then the differential PMOS is used as input for second stage and the second stage is made up of folded cascade configuration. Second stage is

designed as such to increase the open loop gain and also to adjust the common mode voltage of op-amp [9]. The input common mode voltage of VIN+ and VIN- is designed at 0.6V. The third stage is there to provide a high gain. Finally, the last stage have VO1 and VO2 as outputs and the output common mode voltage is also designed at 0.6V. The results of CMRR are up to 166.69dB.

III. CONCLUSION

Table I. Comparison

Specification	[9]	[3]	[5]
CMRR	142dB	>150dB	159.9dB
Technology	90nm	180nm	180nm

In this paper, basics of instrumentation amplifier and also some methods to improve CMRR have been discussed. Three different methods are described to attain high CMRR. In the first method AC coupling is described which results in CMRR of 142dB. Second method describes the use of non overlapping clock to increase CMRR upto 150dB. Last method specifies the use of current mirrors to provide matching and to reduce the cost of overall circuitry which eventually leads to high CMRR of about 159.9dB.A comparison table of the three methods discussed is shown above.

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